FIG. 1

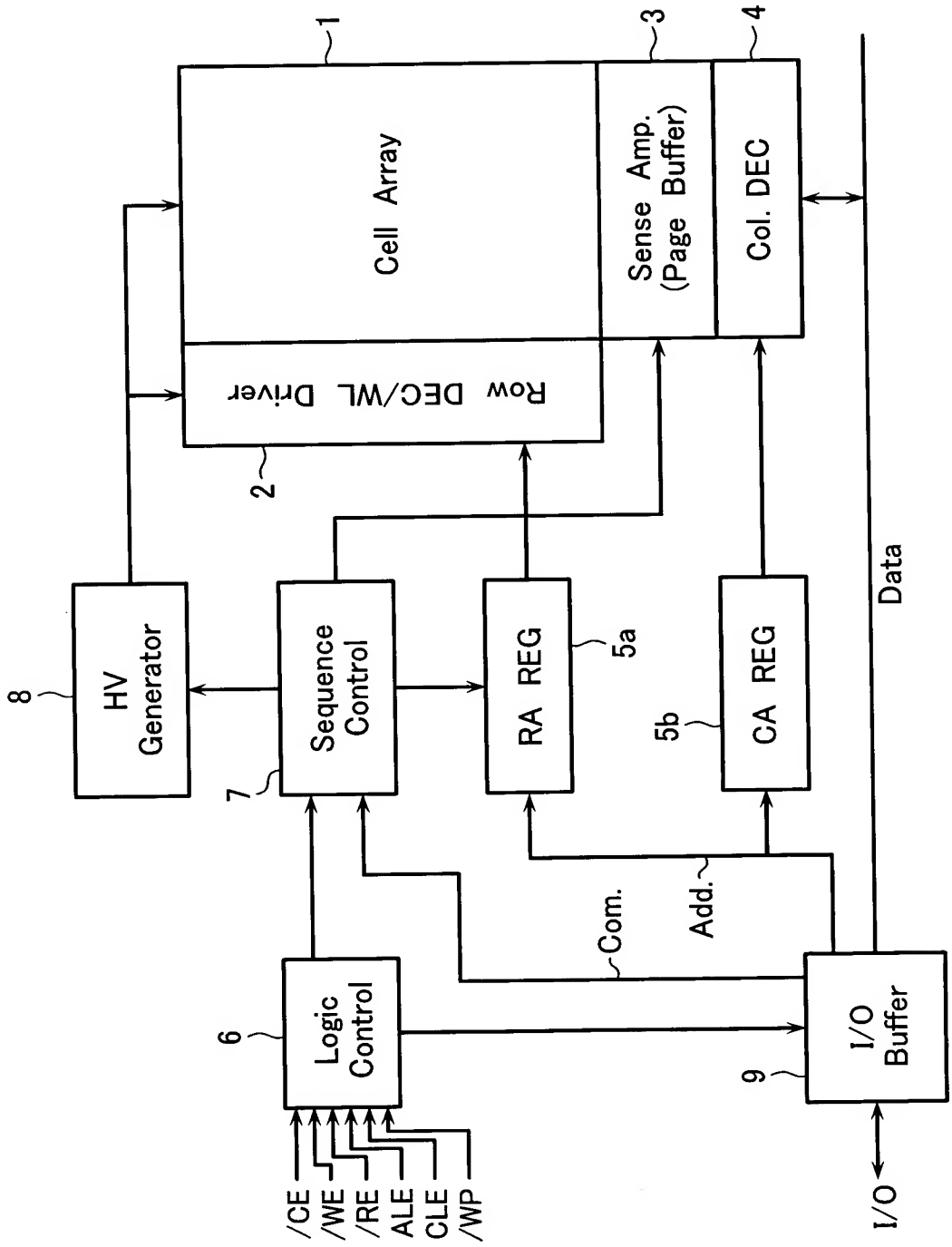

1
3
4
Cell Array
Sense Amp. (Page Buffer)
Col. DEC
Row DEC/WL Driver
2
Data
8
HV Generator
Sequence Control
7
RA REG
5a
5b
CA REG
Com.
Add.
6
Logic Control
9
I/O Buffer
/CE
/WE
/RE
ALE
CLE
/WP
I/O

FIG. 2

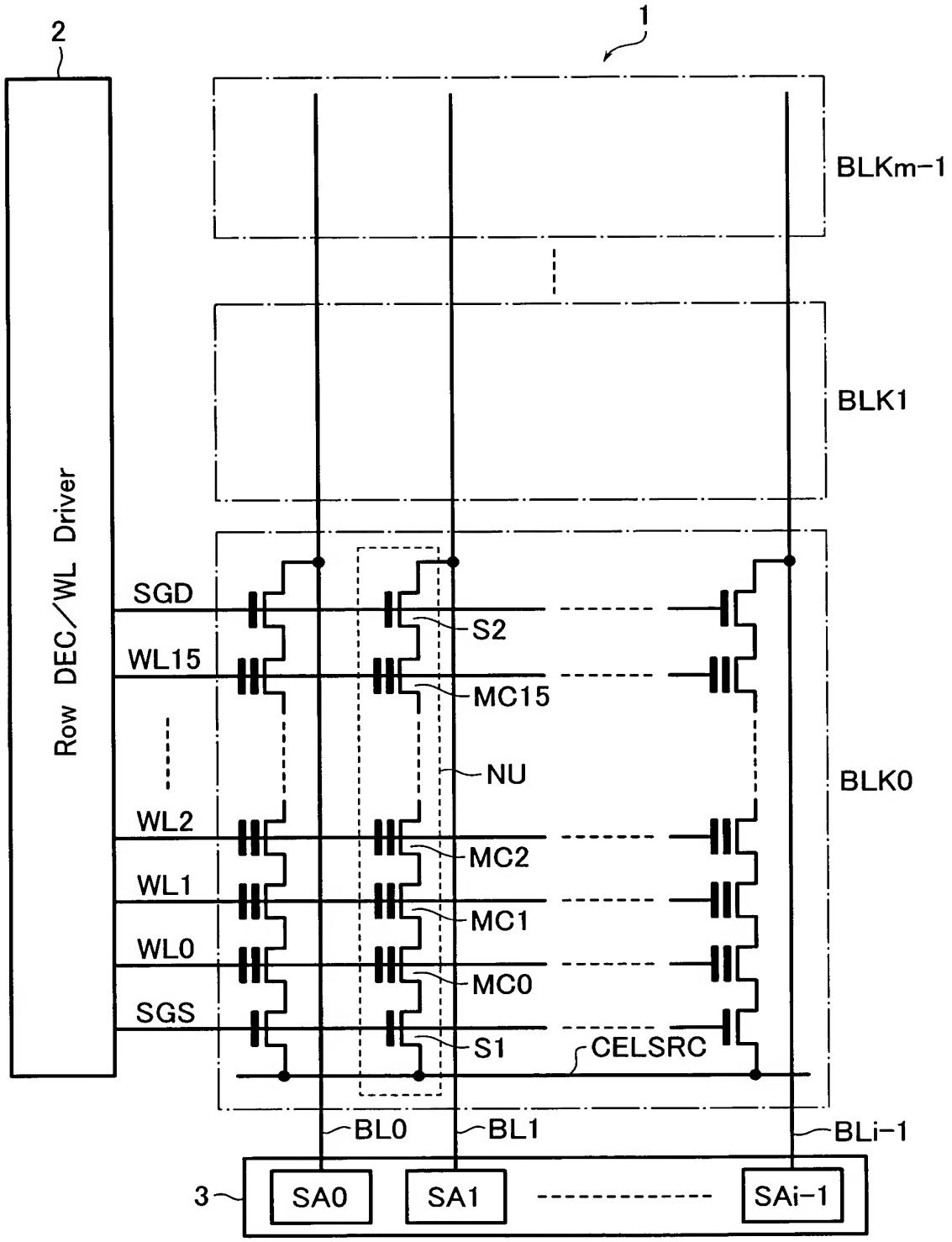
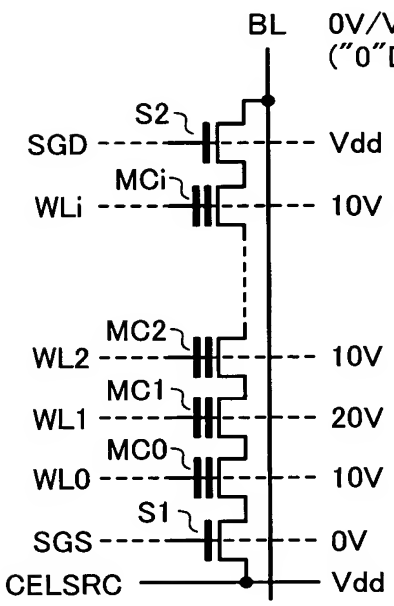

1
2
Row DEC/WL Driver
BLKm-1
BLK1
BLK0
SGD
WL15
WL2
WL1
WL0
SGS
S2
MC15
NU
MC2
MC1
MC0
S1
CELSRC
BL0
BL1
BLi-1
3
SA0
SA1
SAi-1

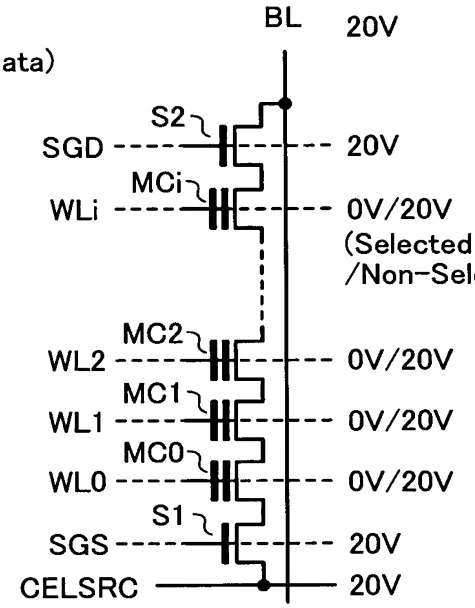
FIG. 3A



Cell Well 0V

[Program]

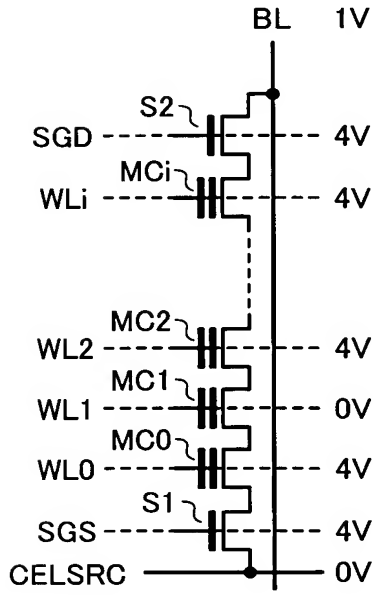
FIG. 3B



Cell Well 20V

[Erase]

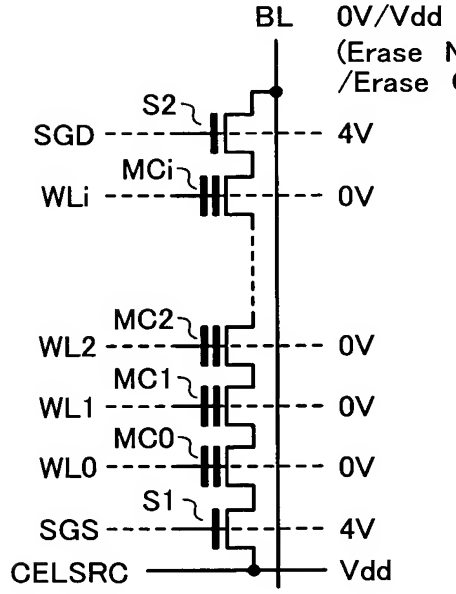
FIG. 3C



Cell Well 0V

[Read]

FIG. 3D



Cell Well 0V

[Erase Verify Read]

FIG. 4A

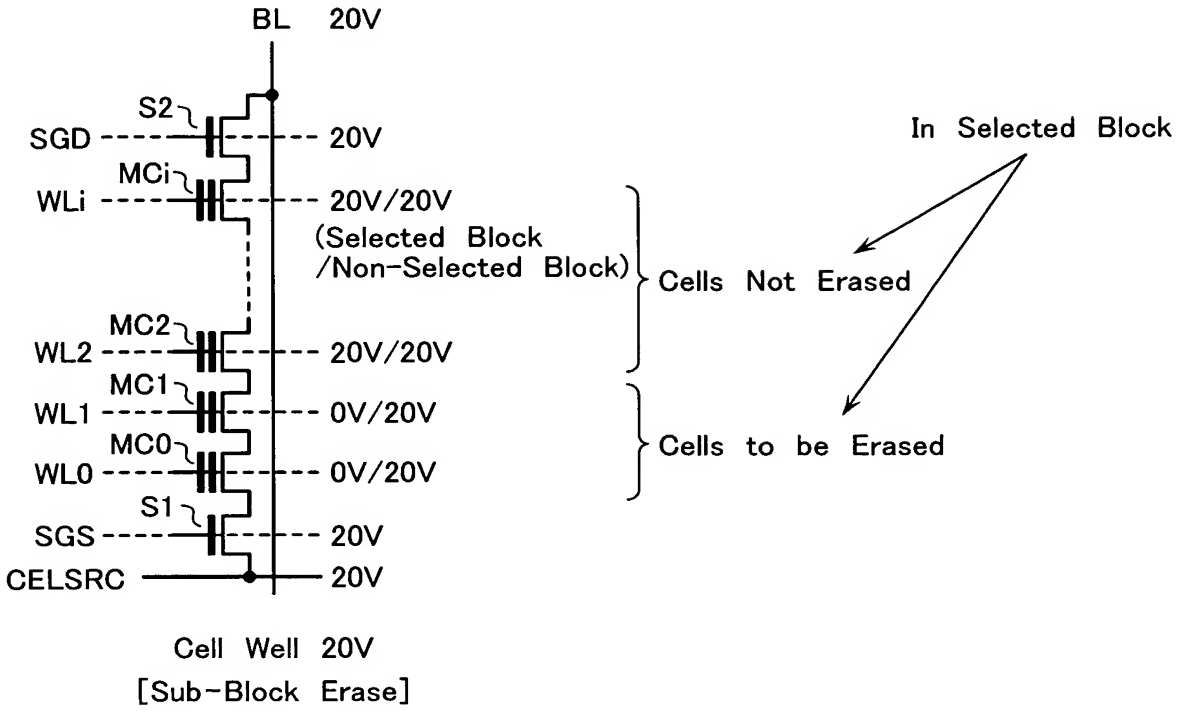


FIG. 4B

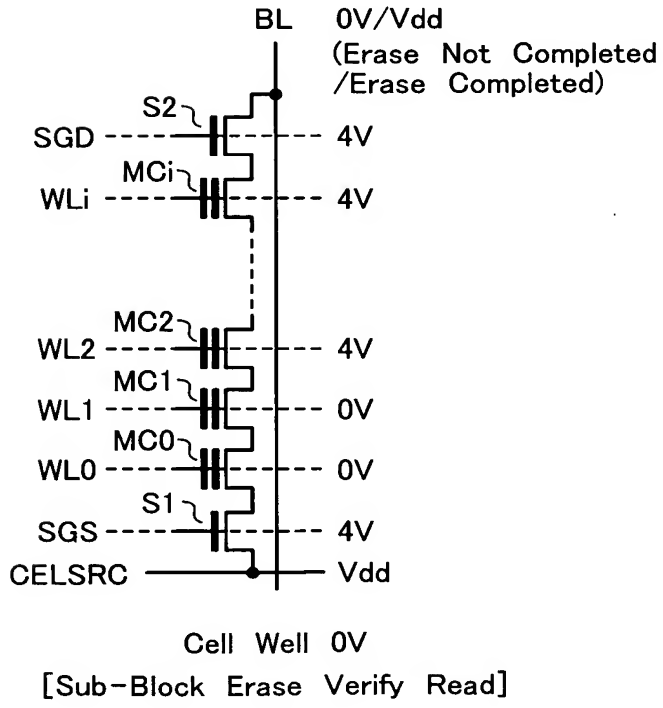


FIG. 4C

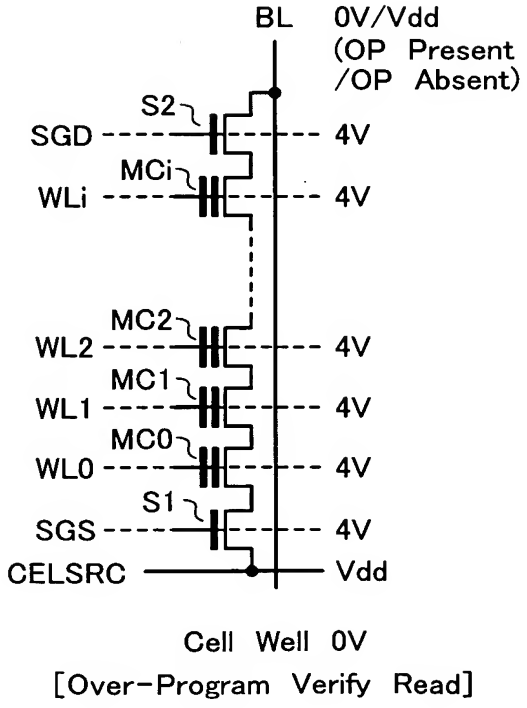


FIG. 5

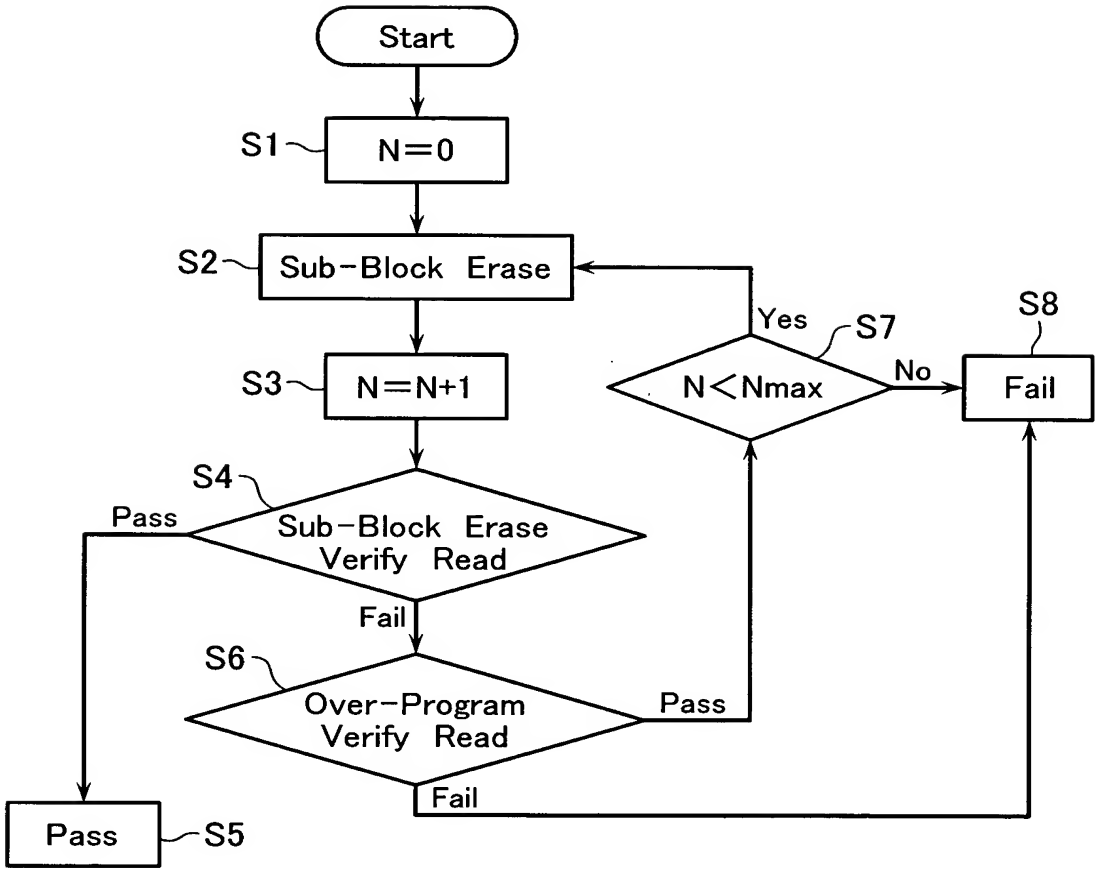

Start
S1
N=0
S2
Sub-Block Erase
S3
N=N+1
S4
Sub-Block Erase Verify Read
Pass
Fail
S6
Over-Program Verify Read
Pass
Fail
Pass
S5
Yes
S7
N<Nmax
No
S8
Fail

FIG. 6

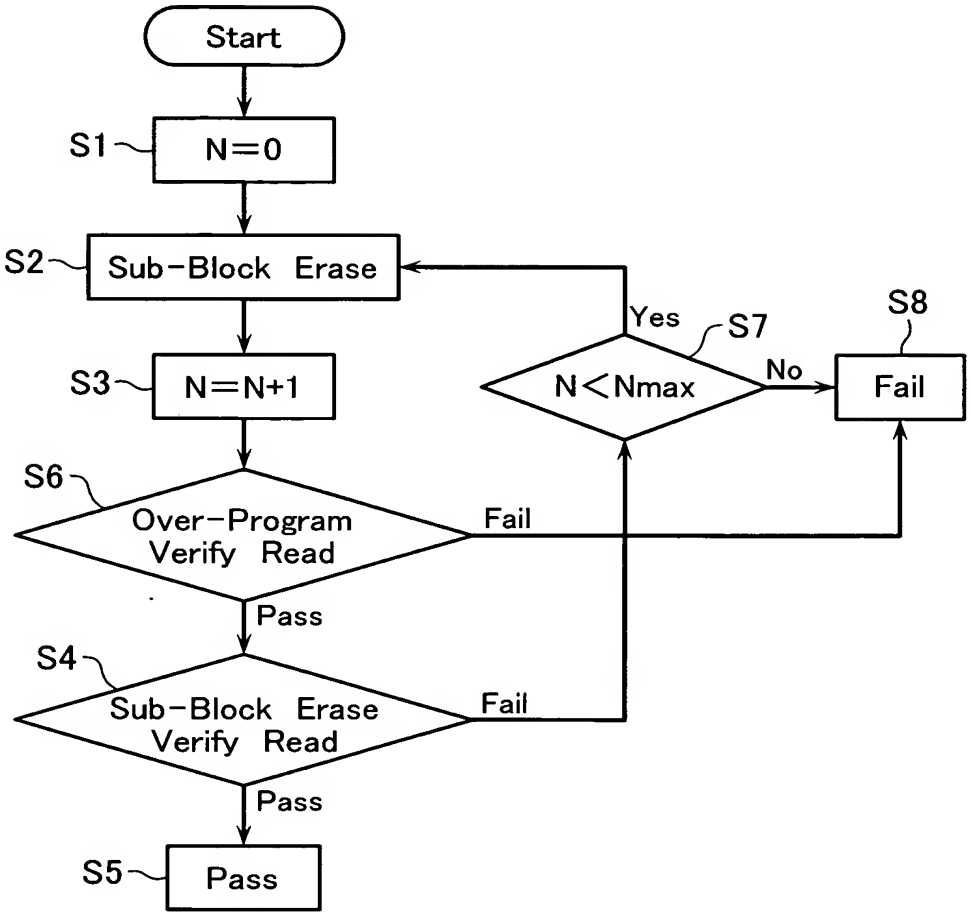

Start
S1
N=0
S2
Sub-Block Erase
S3
N=N+1
S6
Over-Program Verify Read
Fail
Pass
S4
Sub-Block Erase Verify Read
Fail
Pass
S5
Pass
Yes
S7
N<Nmax
No
S8
Fail

FIG. 7

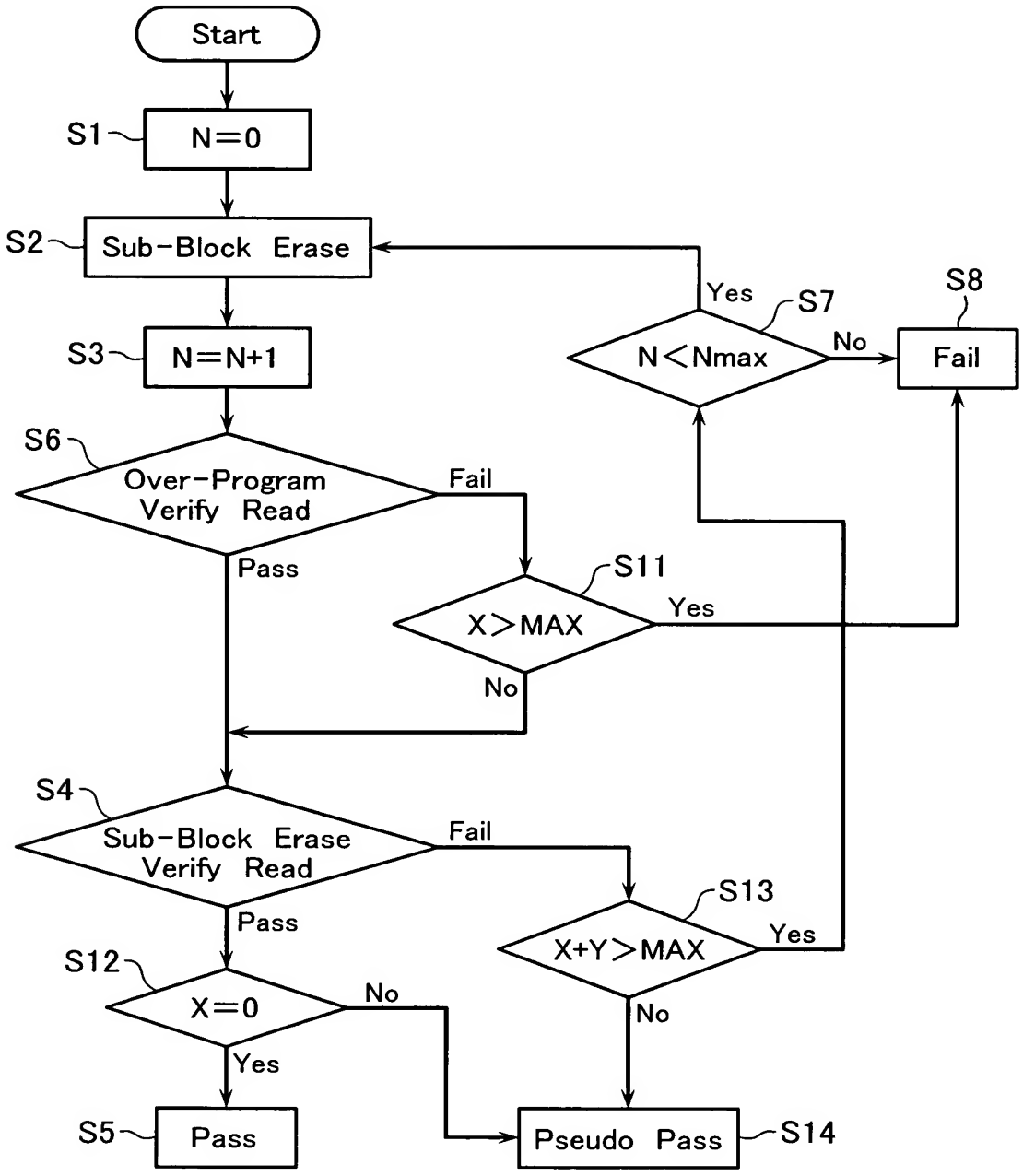

Start
S1
N=0
S2
Sub-Block Erase
S3
N=N+1
S6
Over-Program Verify Read
Fail
Pass
S11
X>MAX
Yes
No
S4
Sub-Block Erase Verify Read
Fail
Pass
S13
X+Y>MAX
Yes
No
S12
X=0
No
Yes
S5
Pass
Pseudo Pass
S14
Yes
S7
N<Nmax
No
S8
Fail

FIG. 8

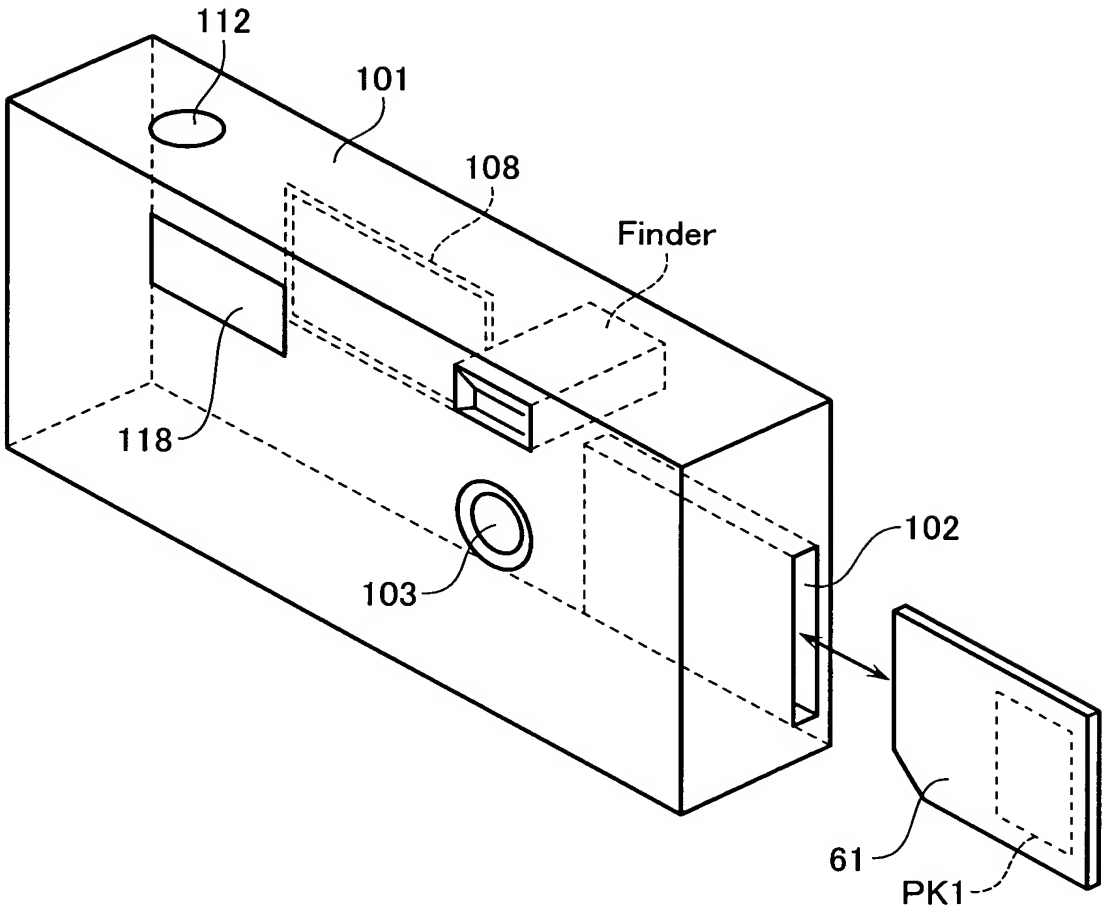


FIG. 9

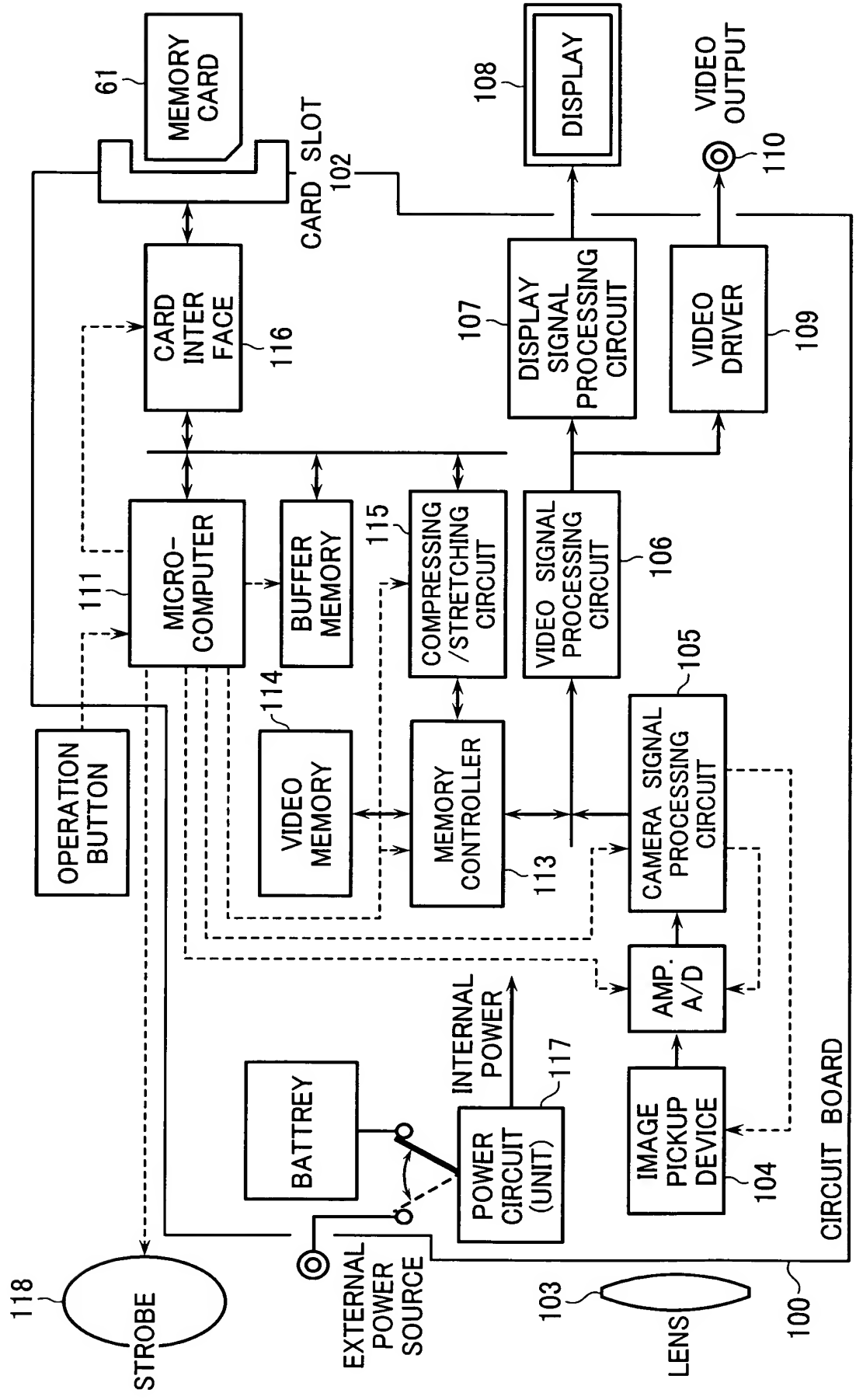

61
MEMORY CARD
CARD SLOT
102
108
DISPLAY
VIDEO OUTPUT
110
CARD INTER FACE
116
107
DISPLAY SIGNAL PROCESSING CIRCUIT
VIDEO DRIVER
109
111
MICRO-COMPUTER
BUFFER MEMORY
115
COMPRESSING /STRETCHING CIRCUIT
VIDEO SIGNAL PROCESSING CIRCUIT
106
105
OPERATION BUTTON
114
VIDEO MEMORY
MEMORY CONTROLLER
113
CAMERA SIGNAL PROCESSING CIRCUIT
AMP. A/D
INTERNAL POWER
117
BATTREY
POWER CIRCUIT (UNIT)
IMAGE PICKUP DEVICE
104
CIRCUIT BOARD
118
STROBE
EXTERNAL POWER SOURCE
103
LENS
100

FIG. 10A

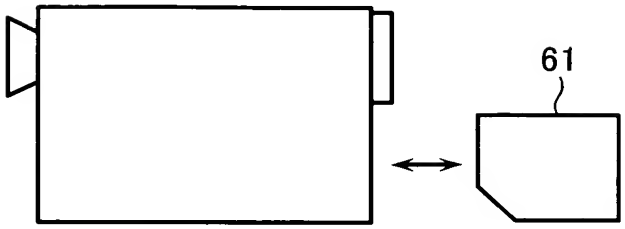


FIG. 10B

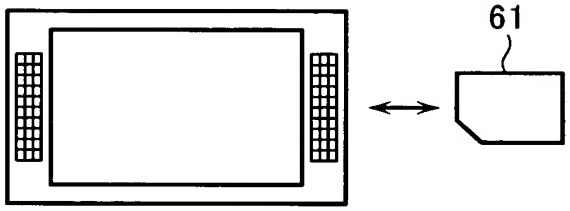


FIG. 10C

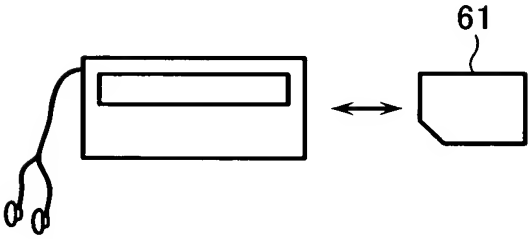


FIG. 10D

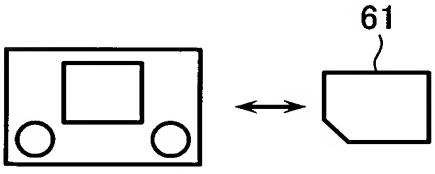


FIG. 10E

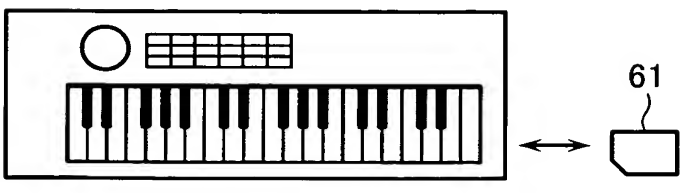


FIG. 10F

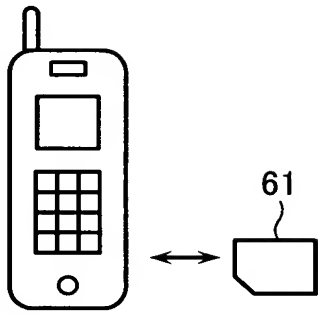


FIG. 10G

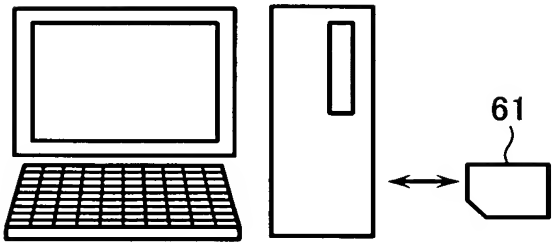


FIG. 10H

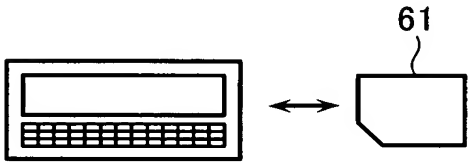


FIG. 10I

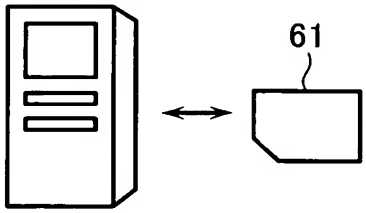


FIG. 10J

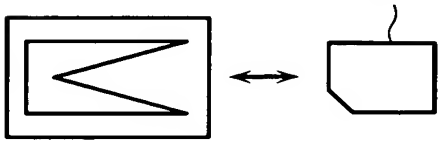


FIG. 11

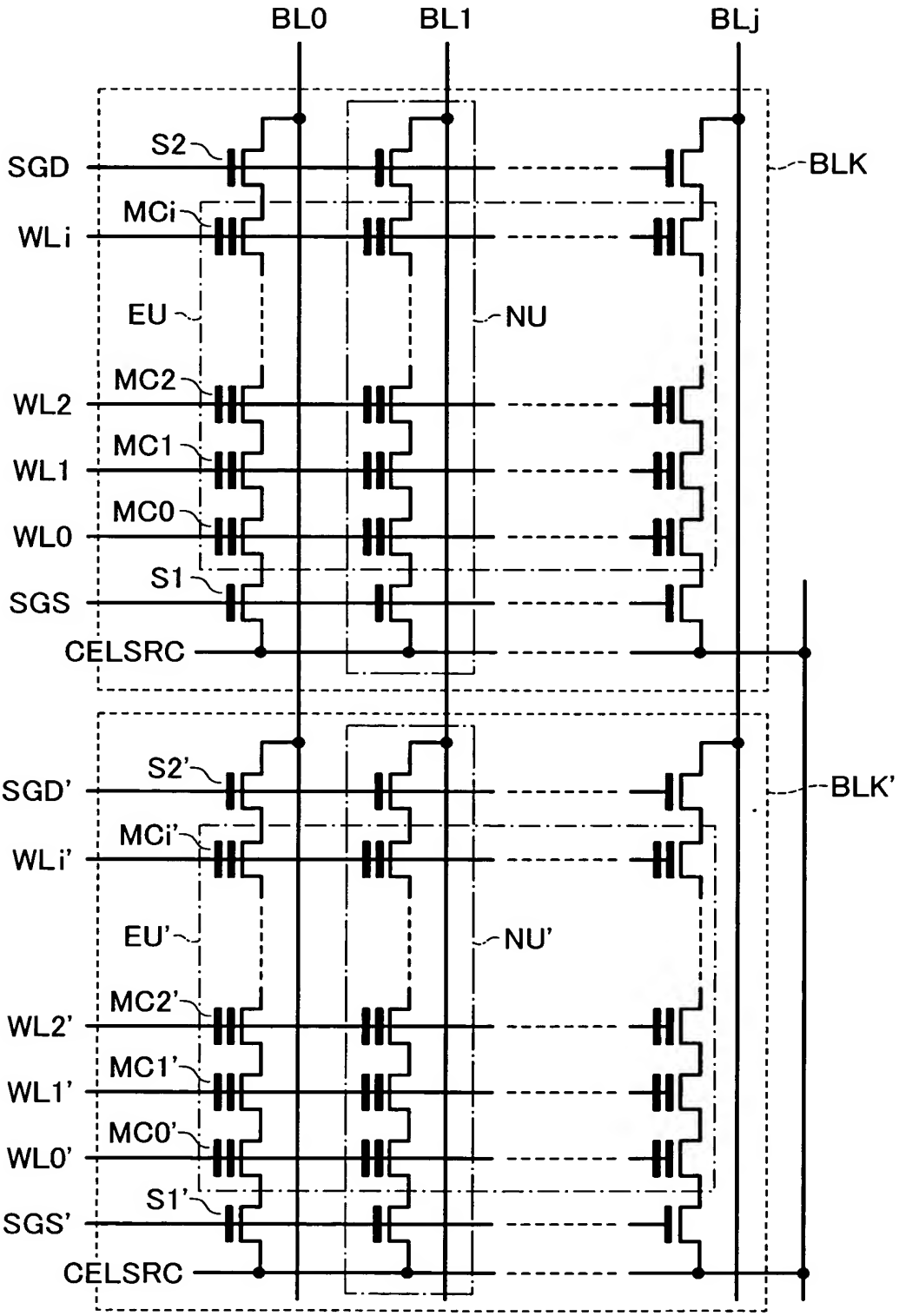
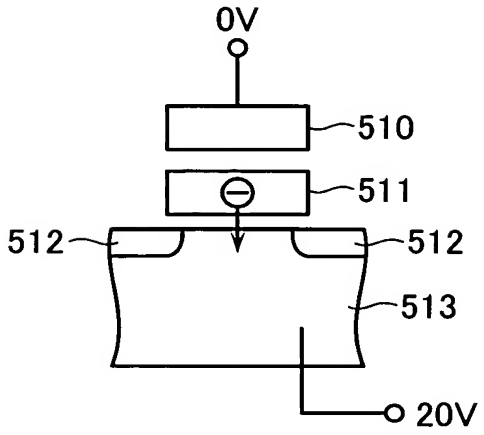
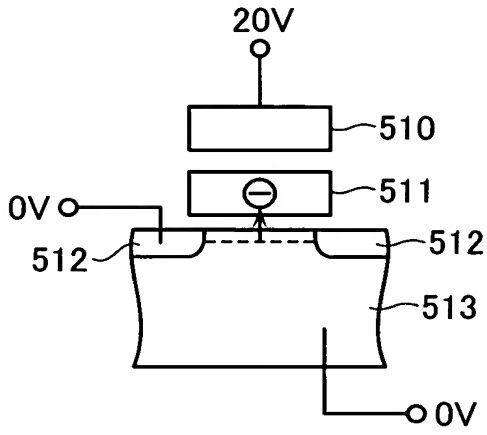

BL0
BL1
BLj
S2
SGD
MCi
WLi
BLK
EU
NU
MC2
WL2
MC1
WL1
MC0
WL0
S1
SGS
CELSRC
S2'
SGD'
MCi'
WLi'
BLK'
EU'
NU'
MC2'
WL2'
MC1'
WL1'
MC0'
WL0'
S1'
SGS'
CELSRC

FIG. 12A



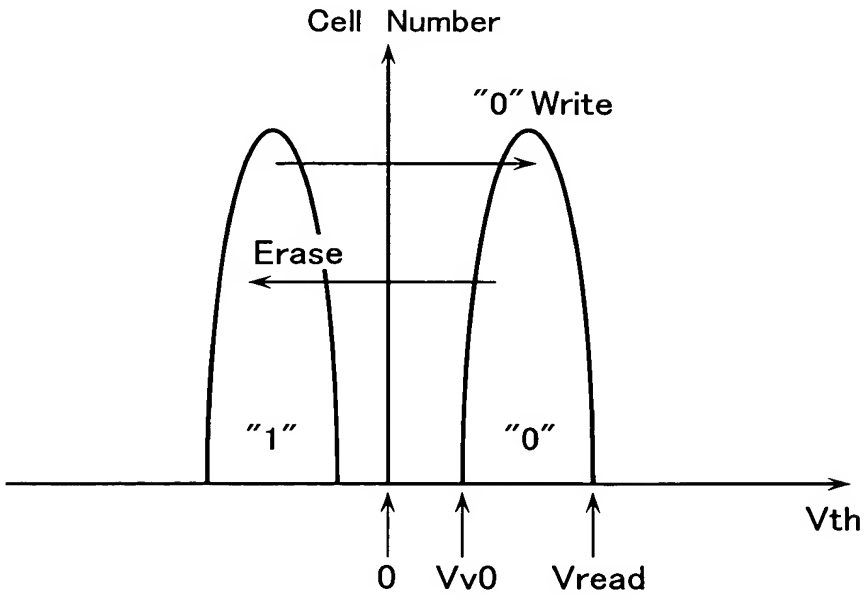
[During Erase]

FIG. 12B



[During Write]

FIG. 12C



[Cell Array Threshold Voltage Distribution]